Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **VOUT**
2. **VOUT**
3. **VOUT**
4. **VOUT**
5. **ADJ**
6. **GND**
7. **EN**
8. **VIN**
9. **VIN**
10. **VIN**

**.047”**

**1**

**2**

**3**

**4**

**10**

**9**

**8**

**7**

**5 6**

**.073”**

**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: .004” x .004” min.**

**Backside Potential:GND**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .047” X .073” DATE: 12/1/22**

**MFG: SILICON SUPPLIES THICKNESS .012” P/N: SiS5219A**

**DG 10.1.2**

#### Rev B, 7/19/02